Ahmed Abdelazeem

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Education

- **Zagazig University, Faculty of Engineering** — Zagazig, Egypt
  Bachelor of Electronics and Communications Engineering; GPA: 3.2 — *July 2016 - June 2021*
  Courses: *Electric Circuits, Electronic Devices and Circuits, Logic Design, Signal and Systems, CMOS Integrated Circuits, Computer Organization and Architecture, VLSI Modeling and Design*

Skills Summary

- **Languages**: C, Python, MATLAB, TCL
- **HDL(RTL)**: Verilog, VHDL
- **Logic Synthesis**: DC(Synopsys), Genus(Cadence)
- **Place & Route**: ICC (II)(Synopsys), Innovus(Cadence)
- **Signoff tools**: StarRC, PrimeTime, Calibre, Virtuoso
- **Other Tools**: HSpice, Vivado, VCS, QuestaSim.
- **Physical Verification**: LVS, DRC, Density rules
- **Technologies**: Linux, GitHub, Git, LaTeX

Experience

- **TRYSL TECH** — KAUST, Saudi Arabia
  ASIC Design Engineer — *Jan 2023 - Present*
  - **Responsible for Physical Implementation of an IP and Chip Level using 65/45/28/14nm**: starting from Netlist to GDS, including floorplanning, Placement, Clock design, Optimization, Routing, Parasitic Extraction, Static Timing Analysis, IR drop analysis, Physical Verification, and Sign-Off.
  - **Work closely with RTL designers**: to debug and root-cause Physical Implementation issues related to design, tools, etc. and arrive at a feasible solution through the augmentation of input and design collateral.
  - **Experience with Synopsys design tools, flows and methodology**: using VCS, Design Compiler, Formality, ICC/ICC2, PrimeTime, PrimePower, StarRC, and ICV, and ICVWB.
- **Center of Nanoelectronics and Devices (CND) @ AUC** — Online
  ASIC Design Engineer — *Feb 2024 - May 2024*
  - **Mentored and Guide a core of 5+ TAs for CDN program.**:
  - **ASIC Design flow**: Guided (TAs) in overseeing the entire ASIC project lifecycle from RTL to GDS, encompassing comprehensive verification, physical design, and timing closure using Synopsys suite tools such as VCS, DC, FM, ICC2, PT/PP, StarRC, and ICV.
- **National Telecommunicarion Institute(NTI)** — New Administrative Capital
  ASIC Design Engineer — *Jun 2023 - Sep 2023*
  - **Mentored and guided 20 students through complete ASIC Design Program**: Developed and delivered tailored instructional material, including presentation slides and hands-on lab exercises, utilizing industry-standard Synopsys tools.
  - **Equipped students with expertise in ASIC Physical Design flow**: including Netlist generation, Floorplanning, Placement, CTS, Routing, and signoff stages (LVS, DRC, Timing, Power), fostering practical skills for success in the semiconductor industry.
- **Summer Intern @ICpedia** — Remote
  ASIC Physical Design — *Jul 2022 - Sep 2022*
  - **Responsible for Physical Implementation of an IP-**: starting from Netlist to GDS, including floorplanning, Placement, Clock design, Optimization, Timing closure, DRC/LVS, LEC, ERC, and sign-off.
- **Military Conscription, Benha Electronics Co.** — Benha
  FPGA Design Engineer — *Dec 2021 - Dec 2022*
  - **Design real-time digital signal processing systems**: Been a part in designing, verification for FPGA development and quality checking large-scale complicated projects of the Air Defense Forces Research and Development department.
  - **Analyze cost and risk factors involved in system development activities**: Contacted suppliers and compared pricings, followed strict deadlines.
- **Summer Intern @Synopsys** — Remote
  ASIC Physical Design Engineer — *Apr 2021 - Apr 2021*
  - **Design Compiler**: Had basic training in DC Shell and also had a beginner level session on the Synthesis flow.
  - **IC Compiler**: Did the entire PNR flow for the ORCA TOP chip using "SAED 32/28nm PDK" with 50K - 60K gates and operates at 60MHz frequency. and also have worked on PrimeTime for learning the basics of STA and to understand how to read the timing reports and how to clear timing violations.
- **Winter Camp @Cadence.** — Remote
  ASIC Physical Design Engineer — *Jan 2021 - Feb 2021*
  - **1-Day hands-on workshop**: to learn the basic concepts of static timing analysis.
  - **2-Days hands-on workshop**: to learn and run complete synthesis flow on a design with the given specifications and optimize it for area, timing, and power with Cadence Genus Synthesis.

- **3-Days hands-on workshop**: to learn how to use the Innovus Implementation System to perform placement, clock tree synthesis, and routing.

- **Winter Camp @Arm Ltd.** Remote
  ASIC Design Engineer *Dec 2020 - Dec 2020*
  - **5-Day hands-on workshop**: to develop Arm Cortex-M0 based SoCs, from creating high-level functional specifications to design, implementation, and testing on FPGA platforms using standard hardware description and software programming languages.

- **Summer Intern @One Lab.** Cairo
  ASIC Design Engineer *Aug 2020 - Nov 2020*
  - **RTL to GDSII**: going through digital design flow starting from Constraint, Synthesis, PnR steps, Timing, Sign off, and Physical verification. Making sure to meet timing, power and physical specifications until the design is clean to be fabricated.

Projects

- **High-Speed Microcontroller for Display intensive Application, GP**: I was responsible for the complete physical design of 180nm Digital Top block and also to IP harden the CORTEX-M0 sub chip. Did the entire PnR flow using Cadence Encounter for the same and also the STA using PrimeTime and physical verification for both the hardened IP and Digital Top block. Sep 2020 - July 2021
- **Mini Stereo Digital Audio Processor (MSDAP) Chip Design**: Developed Verilog RTL code for high speed, low power MSDAP- ASIC chip using Xilinx ISE consisting of a Controller, ALU, Memories and serial communication unit, and verified the system functionality in C. aslo I synthesized the design in Design Compiler & Performed pre-layout simulation in Modelsim. And also developed Final Physical Design using the IC Compiler, Performed Clock Tree Synthesis, Optimization, Parasitic (RC) extraction, Static Timing Analysis (STA). Jan 2021 - Mar2021
- **Implementation of UART Protocol in 6-stage FSM**: Complete the Digital Design Flow from the RTL2GDS using 45nm Free PDK. synthesized the verilog code using DC Compiler, and aslo did the entire PnR flow using Synopsys IC Compiler.
- **Implementation of 16-bits MIPS Processor with 400 MHZ Frequency**: Complete the Digital Design Flow from the RTL2GDS using 45nm Free PDk, with 10 metal layers. Synthesized the verilog code using DC Compiler, and aslo did the entire PnR flow using Synopsys IC Compiler. Performed Clock Tree Synthesis, Optimization, Parasitic (RC) extraction using PrimeTime, Static Timing Analysis (STA). Jan 2021 - Mar2021
- **SoC Implementation of OpenMSP430 Microcontroller**: Complete the physical design of low power microcontroller based on an openMSP430 architecture using 90nm SAED PDK. Dec 2021 - Jan 2022

COURSES

- **C Programming** Udemy,2017
- **Hardware Modeling using Verilog by Prof. Indranil Sengupta** YouTube,2018
- **Introduction to FPGA Design for Embedded Systems** Coursera,2018
- **CMOS Analog IC Design** Mahara-Tech ,2019
- **VLSI CAD Part II: Layout** Coursera,2019
- **Python and Data Structures** Coursera,2020
- **Digital VLSI Design (RTL2GDS) by Prof. Adam Teman.** YouTube,2020
- **VLSI Physical Design by Prof. Indranil Sengupta** Udemy,2020
- **MPU, MCU, SoC and Embedded Systems** YouTube

Volunteer Experience

- **Former Project Management for Enactus ZU,** Zagazig, Egypt
  Prepare clear and concise reports, proposals, and other written materials of a technical nature. Jan 2019 - Feb 2020

- **Former PR director for Hult Prize Foundation, ZU.** Zagazig, Egypt
  Negotiating and receiving governmental and non-governmental grants up to 40,000 EGP. Jan 2018 - Sep 2018